

10/04/121  
01/11/02



U.S. UTILITY Patent Application

PATENT NUMBER and  
ISSUE DATE

NUM	FILED DATE	CLASS	SUBCLASS	GAU	EXAMINER
100441121	01/11/2002	251	666	2316	<i>Edie E. Lane</i>
INVENTORS: Riley John, Wagner Michael, Fiolstad Joseph					
CONTINUING DATA VERIFIED: THIS APPLN CLAIMS BENEFIT OF 5C/281,059 01/11/2001 <i>jjbe</i>					
FOREIGN APPLICATIONS VERIFIED: <i>jjbe</i>					
PUB-PUB DO NOT PUBLISH <input type="checkbox"/> RESCIND <input checked="" type="checkbox"/>					
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no				ATTORNEY DOCKET NO	
35 USC 110 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no				TESSERA 3.0-299	
Verified and Acknowledged by Examiner's Initials					
TITLE: Stacked microelectronic assemblies and methods of making same.					
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)					

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NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
3/25/14		Assistant Examiner	
ISSUE FEE		Total 2	
Amount Due \$ 1330.00	Date Paid	Print Claim for O.G. 1	
Jasmine Clark Primary Examiner		SHEETS DURING	
PREPARED FOR ISSUE		11 14 3A	
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